

What is claimed is:

1 1. A method of forming a thin film transistor device,
2 comprising the steps of:
3 providing a substrate;
4 using a first reticle and forming a semiconductor island
5 on the substrate;
6 forming an oxide layer on the semiconductor island;
7 forming a metal layer on the oxide layer;
8 using a second reticle and forming a photoresist pattern
9 on part of the metal layer;
10 using the photoresist pattern as a mask and isotropically
11 etching part of the metal layer and part of the oxide
12 layer to form a gate and a gate dielectric layer,
13 wherein the photoresist pattern is wider than the
14 gate and gate dielectric layer, but narrower than
15 the semiconductor island;
16 using the photoresist pattern as a mask and performing a
17 heavy doping ion implantation on the semiconductor
18 island to form a source/drain region in part of the
19 semiconductor island;
20 removing the photoresist pattern; and
21 using the gate as a mask and performing a light doping ion
22 implantation on the semiconductor island to form a
23 lightly doped drain (LDD) region in part of the
24 semiconductor island.

1 2. The method according to claim 1, wherein the substrate
2 is a glass substrate.

1 3. The method according to claim 1, wherein the
2 semiconductor island is a polysilicon layer.

1 4. The method according to claim 1, wherein the oxide
2 layer is a SiO₂ layer.

1 5. The method according to claim 1, wherein the metal
2 layer is an Al, Ti, Ta, Cr, Mo, MoW or alloy of the above layer.

1 6. The method according to claim 1, wherein the method
2 of isotropically etching part of the metal layer and the oxide
3 layer comprises:
4 using a first etchant with a first etching rate to remove
5 part of the metal layer; and
6 using a second etchant with a second etching rate to remove
7 part of the oxide layer;
8 wherein the second etching rate is greater than the first
9 etching rate in order to make the width of the gate
10 dielectric layer smaller than the width of the gate.

1 7. The method according to claim 6, wherein the metal
2 layer is an Al or Ti layer.

1 8. The method according to claim 7, wherein the oxide
2 layer is a SiO₂ layer.

1 9. The method according to claim 8, wherein the first
2 etchant comprises phosphoric acid, acetic acid and nitric acid.

1 10. The method according to claim 8, wherein the second
2 etchant comprises hydrofluoric acid.

1 11. A method of forming a thin film transistor device on
2 a color filter, comprising the steps of:
3 providing a substrate having a light-transmitting area and
4 a capacitor area, wherein the light-transmitting area
5 further includes an active area;
6 forming a first metal layer on the substrate;
7 using a first reticle and removing part of the first metal
8 layer to form a hole exposing the substrate in the
9 light-transmitting area, wherein the first metal
10 layer in the capacitor area serves as a lower electrode
11 of a capacitor;
12 filling a pigment into the hole to form a color filter on
13 the substrate;
14 forming a first buffer layer on the color filter and the
15 metal layer;
16 using a second reticle and forming a semiconductor island
17 on the first buffer layer in the active area;
18 forming an oxide layer on the semiconductor island;
19 forming a second metal layer on the oxide layer;
20 using a third reticle and forming a photoresist pattern
21 on part of the second metal layer;
22 using the photoresist pattern as a mask and isotropically
23 etching part of the second metal layer, part of the
24 oxide layer and part of the first buffer layer to
25 expose part of the color filter and part of the first
26 metal layer and thus forming a gate, a gate dielectric
27 layer, an upper electrode of the capacitor and a
28 dielectric layer of the capacitor, wherein the
29 photoresist pattern is wider than the gate and the

30 gate dielectric layer, but narrower than the
31 semiconductor island;
32 using the photoresist pattern as a mask and performing a
33 heavy doping ion implantation on the semiconductor
34 island to form a source/drain region in part of the
35 semiconductor island;
36 removing the photoresist pattern;
37 using the gate as a mask and performing a light doping ion
38 implantation on the semiconductor island to form a
39 lightly doped drain (LDD) region in part of the
40 semiconductor island; and
41 using a fourth reticle and forming a transparent conducting
42 layer on the color filter, wherein the transparent
43 conducting layer electrically connects the
44 source/drain region and the first metal layer.

1 12. The method according to claim 11, further comprising:
2 forming a second buffer layer between the first metal layer
3 and the substrate.

1 13. The method according to claim 11, wherein the first
2 buffer layer is a SiO₂ layer.

1 14. The method according to claim 12, wherein the second
2 buffer layer is a SiO₂ layer.

1 15. The method according to claim 11, wherein the
2 semiconductor island is a polysilicon layer.

1 16. The method according to claim 11, wherein the second
2 metal layer is an Al, Ti, Ta, Cr, Mo, MoW or alloy of the above
3 layer.

1 17. The method according to claim 11, wherein the method
2 of isotropically etching part of the second metal layer and part
3 of the oxide layer comprises:

4 using a first etchant with a first etching rate to remove
5 part of the second metal layer; and

6 using a second etchant with a second etching rate to remove
7 part of the oxide layer;

8 wherein the second etching rate is greater than the first
9 etching rate in order to form the width of the gate
10 dielectric layer smaller than the width of the gate.

1 18. The method according to claim 17, wherein the second
2 metal layer is an Al or Ti layer.

1 19. The method according to claim 18, wherein the oxide
2 layer is a SiO₂ layer.

1 20. The method according to claim 19, wherein the first
2 etchant comprises phosphoric acid, acetic acid and nitric acid.

1 21. The method according to claim 19, wherein the second
2 etchant comprises hydrofluoric acid.

1 22. The method according to claim 11, wherein the pigment
2 is red, green or blue.

1 23. The method according to claim 11, wherein the
2 transparent conducting layer is an indium tin oxide (ITO) or
3 indium zinc oxide (IZO) layer.